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EXAMINER

BERHANE, YOSIEF H

ART UNIT	PAPER NUMBER
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2419

MAIL DATE	DELIVERY MODE
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02/04/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/567,206	Applicant(s) PHILIPS ET AL.	
	Examiner YOSIEF BERHANE	Art Unit 2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 03 February 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02/03/2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-10 have been examined and are pending.

Information Disclosure Statement

2. An initialed and dated copy of Applicant's IDS form 1449 submitted 2/03/2006, is attached to the instant Office action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 10 recites "computer readable medium" which is not disclosed in the specification as originally filed.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

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Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claim 10 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 10 discloses a "computer readable medium", where the closest reference to a "computer readable medium" in the original specification is on page 20, lines 26-33, which discloses "data on a carrier" where the carrier includes "data traveling over a network connection- wired or wireless" or "program code on paper", both of which are non-statutory subject matter. Thus the medium as claimed is non-statutory for the aforementioned reason.

Response to Arguments:

On page 6 of Applicants Response, with regards to claim 1-4 and 9-10, applicant argues: independent claims 1 and 9 and amended independent claim 10 recite determining a filling measurement (mF) of an amount (F) of data units in the buffer (102) at a specified time instant (TI) and controlling the delay (A) by controlling the data rate conversion component (108) on the basis of the filling measurement (mF) and the input time measurement (mTa), which are not disclosed in Williams et al. Therefore, independent claims 1 and 9 and currently amended independent claim 10 should be found allowable, and such action is respectfully requested.

The examiner respectfully disagrees with applicants arguments because Williams teaches a filling measurement of an amount of data units in the buffer at a specified time

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instant (Col. 5, lines 51-55, a controller that continuously monitors a buffer data level, i.e., the amount of data in the buffer from moment to moment and buffer fill rate 54, i.e., the rate at which data is filling buffer. Note, Williams discloses that the controller monitors the buffer fill from moment to moment, thus at a specified time instant)

and controlling the delay by controlling the data rate conversion component on the basis of the filling measurement and the input time (col. 7, lines 9-12, Williams discloses that a controller maintains buffer data level (claimed filling measurement) between lower and upper limiting data-level thresholds by causing variations in the source (claimed input time measurement) or sink data rate as required. Note, as disclosed in Fig.1, and Col. 3, lines 31-35, the controller controls and regulates the flow of data through data rate/flow regulator thereby being under the control of the data rate/flow regulator).

On page 8 of Applicants Response, with regards to claims 5-8, applicant argues: Applicants respectfully assert that Williams et al. reference fails to support a *prima facie* case of obviousness because, the cited reference fails to teach or suggest all of the elements of the Applicants' invention, such as "data rate conversion component (108), arranged to set a ratio of the read rate (R_r) and the write rate (R_w), on the basis of the filling measurement (mF)", "input time measuring component (112) is comprised, arranged to measure an input time instant (T_a) of input of the data unit (150) in the buffer management system (100), and yielding an input time measurement (mT_a)", and "controlling the delay (A) by controlling the data rate conversion component (108) on the basis of the filling measurement (mF) and the input time measurement (mT_a)".

The examiner respectfully disagrees with Applicants arguments, because Williams teaches a data rate conversion component (Fig.1, box 38, controller), arranged to set a ratio of the read rate and the write rate, on the basis of the filling measurement (col. 7, lines 9-12, Williams discloses that a controller maintains buffer data level between lower and upper limiting data-level thresholds by causing variations in the source or sink data rate as required. Williams further discloses in col. 7, lines 15-18, when buffer data level is decreasing and approaching lower limiting data-level threshold, the controller causes buffer fill rate to become positive. Note, as defined in Col. 6, lines 61-61, a positive buffer fill rate means the source data rate is greater than the sink data rate. Thus, based on the buffer data level (claimed filling measurement) the controller portions the amount of source rate and sink rate (claimed write rate and read rate), thereby setting a ratio.);

Williams teaches input time measuring component (Fig. 1, box 30, Input) is comprised, arranged to measure an input time instant of input of the data unit in the buffer management system (Col. 4, lines 52-54, Williams discloses that an input function of data-rate regulator receives data and writes data to buffer at the source data rate.), and yielding an input time measurement (Col. 4, lines 52-54, source data rate);

Williams teaches controlling the delay (Fig. 1, box 26, flow of data controlled by a Data Rate Regulator. Note, the data is buffered at box 36, thus the data is delayed) by controlling the data rate conversion component on the basis of the filling measurement and the input time measurement (col. 7, lines 9-12, Williams discloses that a controller maintains buffer data level (claimed filling measurement) between lower and upper limiting data-level thresholds by causing variations in the source (claimed input time

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measurement) or sink data rate as required. Note, as disclosed in Fig.1, and Col. 3, lines 31-35, the controller controls and regulates the flow of data through data rate/flow regulator thereby being under the control of the data rate/flow regulator).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 6, and 9-10 are rejected under 35 U.S.C. 102(e) patented on 03/30/2004 as being anticipated by US patent 6715007 to Williams et al. (hereinafter “Williams”).

As per claim 1, Williams teaches buffer management system (Fig. 1, Box 22, Data Rate Regulator) for controlling, in a data communication system (Williams discloses, Col. 2, lines 27-30, as well as FIG. 1, a block diagram depicting a communication system incorporating a data-rate regulator),

a delay of a data unit (Fig. 1, box 26, flow of data controlled by a Data Rate Regulator. Note, the data is buffered at box 36, thus the data is delayed)

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between input in the buffer management system (Fig. 1, box 30, Input) and output from the buffer management system (Fig.1, box 34, Output), comprising (Col. 3, lines 31-35, as well as Fig. 1, Williams discloses that a controller is used to control and regulate the flow of data between data source and data sink via the data rate/flow regulator. Note, as can be shown by Fig.1, the data rate/flow regulator is used to control data flow between data source and data sink):

a buffer (Fig.1 box, 36, Buffer), in which blocks of inputted data units are written with a block write rate (Col. 3, lines 18-20, Williams discloses that Data is received in data-rate regulator by an input function and written into a buffer at the source data rate.),

and from which data units are read with a read rate (Col. 3, lines 23-25, Williams discloses that data is read from the buffer at a sink rate.);

a buffer filling measurement component (Fig. 1, box 38, Controller)

arranged to determine an amount of data units in the buffer at a specified time instant (Col. 5, lines 51-55, a controller that continuously monitors a buffer data level, i.e., the amount of data in the buffer from moment to moment and buffer fill rate 54, i.e., the rate at which data is filling buffer. Note, Williams discloses that the controller monitors the buffer fill from moment to moment, thus at a specified time instant),

and yielding a filling measurement (FIG. 2 shows a schematic view depicting a data-rate regulation buffer with a diagram of buffer level over time. Note, the diagram in fig. 2, shows the fill level of the buffer at a given time instant, thus the buffer yields a fill measurement);

and a data rate conversion component (Fig.1, box 38, controller), arranged to set a ratio of the read rate and the write rate, on the basis of the filling measurement (col. 7,

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lines 9-12, Williams discloses that a controller maintains buffer data level between lower and upper limiting data-level thresholds by causing variations in the source or sink data rate as required. Williams further discloses in col. 7, lines 15-18, when buffer data level is decreasing and approaching lower limiting data-level threshold, the controller causes buffer fill rate to become positive. Note, as defined in Col. 6, lines 61-61, a positive buffer fill rate means the source data rate is greater than the sink data rate. Thus, based on the buffer data level (claimed filling measurement) the controller portions the amount of source rate and sink rate (claimed write rate and read rate), thereby setting a ratio.);

characterized in that an input time measuring component (Fig. 1, box 30, Input) is comprised, arranged to measure an input time instant of input of the data unit in the buffer management system (Col. 4, lines 52-54, Williams discloses that an input function of data-rate regulator receives data and writes data to buffer at the source data rate.),

and yielding an input time measurement (Col. 4, lines 52-54, source data rate);

and a delay control component (Fig.1, box 22, data rate/flow regulator) is comprised for controlling the delay (Col. 3, lines 31-35, as well as Fig. 1, Williams discloses that a data rate/flow regulator incorporates a controller to control and regulate the flow of data between data source and data sink. Note, as disclosed in Col. 3, lines 18-20 and Col. 3, lines 23-25, the process of regulating a data flow includes buffering data at a source rate before transmitting the data at a sink rate, thus the data will be delayed, whereby the data regulator will control the delay)

by controlling the data rate conversion component on the basis of the filling measurement and the input time measurement (col. 7, lines 9-12, Williams discloses that a controller maintains buffer data level (claimed filling measurement) between lower and

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upper limiting data-level thresholds by causing variations in the source (claimed input time measurement) or sink data rate as required. Note, as disclosed in Fig.1, and Col. 3, lines 31-35, the controller controls and regulates the flow of data through data rate/flow regulator thereby being under the control of the data rate/flow regulator).

As per claim 2, Williams teaches buffer management system as claimed in claim 1, comprising a read time measuring component (Fig. 1, box 34, Output), arranged to measure a read time instant of a first data unit (Col. 5, lines 19-21, Williams discloses that an output function of the data-rate regulator reads data from the buffer and transmits data to data sink at the sink data rate),

and yielding a read time measurement (Col. 5, lines 19-21, sink data rate),

and in which buffer management system, the delay control component (Fig.1, box 22, data rate/flow regulator) is arranged to control the data rate conversion component (Fig. 1, box 38, controller) on the basis of the read time measurement (col. 7, lines 9-12, Williams discloses that a controller maintains buffer data level between lower and upper limiting data-level thresholds by causing variations in the source or sink data rate (claimed read time measurement) as required. Note, as disclosed in Fig.1, and Col. 3, lines 31-35, the controller controls and regulates the flow of data through data rate/flow regulator thereby being under the control of the data rate/flow regulator).

As per claim 3, Williams teaches buffer management system as claimed in claim 1, in which the data rate conversion component comprises a voltage controlled oscillator (Col. 1, lines 25-30, Williams discloses that it is well known in the art to utilize high accuracy data source and data sink crystal oscillators. Also, Col. 10, lines 23-24,

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Williams discloses that in a desired embodiment, a source and sink data rate may be produced by a crystal oscillator and a digital divider).

As per claim 4, Williams teaches buffer management system as claimed in claim 1, in which the data rate conversion component comprises a sample rate converter, arranged to produce a second number of samples out of a first number of samples (col. 5 lines 65-67 and col. 6, lines 1-2, Williams discloses that a controller (claimed data rate conversion component) may monitor buffer data level by sampling. Note; sampling requires that a second number of samples are produced by a first number of samples.).

As per claim 6, Williams teaches digital audio receiver comprising (Fig. 1, Box 58, Receiver. Note, Col. 10, 40-47, Williams discloses that the present invention teaches a method of regulating a flow of data in a communication system and an apparatus therefor, a process suitable for use with conventional software-determined radios and other programmable devices, thus radios and other programmable devices in a communication system will include a digital audio receiver.)

a radio reception component with an output (Fig. 1, box 58, Receiver) connected to a buffer management system (Col. 3, lines 39-42, Williams discloses that the data-rate regulator(claimed buffer management system), is physically incorporated into data sink, i.e., is located within a radio receiver of the communication system) as in claim 1.

As per claim 9, Williams teaches method of controlling in a data communication system (Williams discloses, Col. 2, lines 27-30, as well as FIG. 1, a block diagram depicting a communication system incorporating a data-rate regulator)

a delay of a data unit (Fig. 1, box 26, flow of data. Note, the data is buffered at box 36, thus the data is delayed)

between input (Fig. 1, box 30, Input) in a digital audio receiver and output (Fig.1, box 34, Output) from the digital audio receiver, comprising (Col. 3, lines 31-35, as well as Fig. 1, Williams discloses that a controller is used to control and regulate the flow of data between data source and data sink via the data rate/flow regulator. Note, in Col. 10, 40-47, Williams discloses that the present invention teaches a method of regulating a flow of data in a communication system and an apparatus therefor, a process suitable for use with conventional software-determined radios and other programmable devices, thus radios and other programmable devices in a communication system will include a digital audio receiver.):

Writing blocks of inputted data units in a buffer with a block write rate (Col. 3, lines 18-20, Williams discloses that Data is received in data-rate regulator by an input function and written into a buffer at the source data rate.);

Determining a filling measurement of an amount of data units in the buffer at a specified time instant (Col. 5, lines 51-55, a controller that continuously monitors a buffer data level, i.e., the amount of data in the buffer from moment to moment and buffer fill rate 54, i.e., the rate at which data is filling buffer. Note, Williams discloses that the controller monitors the buffer fill from moment to moment, thus at a specified time instant);

Setting a ratio of a read rate and the write rate, on the basis of the filling measurement (col. 7, lines 9-12, Williams discloses that a controller maintains buffer data level between lower and upper limiting data-level thresholds by causing variations in the source or sink data rate as required. Williams further discloses in col. 7, lines 15-18, when buffer data level is decreasing and approaching lower limiting data-level threshold, the controller causes buffer fill rate to become positive. Note, as defined in Col. 6, lines 61-61, a positive buffer fill rate means the source data rate is greater than the sink data rate. Thus, based on the buffer data level (claimed filling measurement) the controller portions the amount of source rate and sink rate (claimed write rate and read rate), thereby setting a ratio);

and reading data units from the buffer with the read rate (Col. 3, lines 23-25, Williams discloses that data is read from the buffer at a sink rate.),

the method being characterized in that: an input time measurement (Col. 4, lines 52-54, source data rate) of an input time instant of input of the data unit in the digital audio receiver is performed (Col. 4, lines 52-54, Williams discloses that an input function of data-rate regulator receives data and writes data to buffer at the source data rate);

and the delay is controlled by setting the ratio of the read rate and the write rate also on the basis of the input time measurement (col. 7, lines 9-12, Williams discloses that a controller maintains buffer data level between lower and upper limiting data-level thresholds by causing variations in the source or sink data rate as required. Williams further discloses in col. 7, lines 15-18, when buffer data level is decreasing and approaching lower limiting data-level threshold, the controller causes buffer fill rate to become positive. Note, as defined in Col. 6, lines 61-61, a positive buffer fill rate means

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the source data rate is greater than the sink data rate. Thus, based on the buffer data level (claimed filling measurement) the controller portions the amount of source rate and sink rate (claimed write and read rate), thereby setting a ratio).

As per claim 10, Williams teaches a computer readable medium having instructions, that when executed by a computing platform, result in execution of a method of controlling in a data communication system (Col. 3, lines 29-31, Williams discloses a Controller, which regulates the flow of data in a communication system, is coupled to and under the control of a control program realized within another portion of controller-readable memory)

a delay of a data unit (Fig. 1, box 26, flow of data. Note, the data is buffered at box 36, thus the data is delayed)

between input (Fig. 1, box 30, Input) in a digital audio receiver and output (Fig. 1, box 34, Output) from the digital audio receiver, comprising (Col. 3, lines 31-35, as well as Fig. 1, Williams discloses that a controller is used to control and regulate the flow of data between data source and data sink via the data rate/flow regulator. Note, in Col. 10, 40-47, Williams discloses that the present invention teaches a method of regulating a flow of data in a communication system and an apparatus therefor, a process suitable for use with conventional software-determined radios and other programmable devices, thus radios and other programmable devices in a communication system will include a digital audio receiver.):

Writing blocks of inputted data units in a buffer with a block write rate (Col. 3, lines 18-20, Williams discloses that Data is received in data-rate regulator by an input function and written into a buffer at the source data rate.);

Determining a filling measurement of an amount of data units in the buffer at a specified time instant (Col. 5, lines 51-55, a controller that continuously monitors a buffer data level, i.e., the amount of data in the buffer from moment to moment and buffer fill rate 54, i.e., the rate at which data is filling buffer. Note, Williams discloses that the controller monitors the buffer fill from moment to moment, thus at a specified time instant);

Setting a ratio of a read rate and the write rate, on the basis of the filling measurement (col. 7, lines 9-12, Williams discloses that a controller maintains buffer data level between lower and upper limiting data-level thresholds by causing variations in the source or sink data rate as required. Williams further discloses in col. 7, lines 15-18, when buffer data level is decreasing and approaching lower limiting data-level threshold, the controller causes buffer fill rate to become positive. Note, as defined in Col. 6, lines 61-61, a positive buffer fill rate means the source data rate is greater than the sink data rate. Thus, based on the buffer data level (claimed filling measurement) the controller portions the amount of source rate and sink rate (claimed write rate and read rate), thereby setting a ratio);

and reading data units from the buffer with the read rate (Col. 3, lines 23-25, Williams discloses that data is read from the buffer at a sink rate.),

the method being characterized in that: an input time measurement (Col. 4, lines 52-54, source data rate) of an input time instant of input of the data unit in the digital

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audio receiver is performed (Col. 4, lines 52-54, Williams discloses that an input function of data-rate regulator receives data and writes data to buffer at the source data rate);

and the delay is controlled by setting the ratio of the read rate and the write rate also on the basis of the input time measurement (col. 7, lines 9-12, Williams discloses that a controller maintains buffer data level between lower and upper limiting data-level thresholds by causing variations in the source or sink data rate as required. Williams further discloses in col. 7, lines 15-18, when buffer data level is decreasing and approaching lower limiting data-level threshold, the controller causes buffer fill rate to become positive. Note, as defined in Col. 6, lines 61-61, a positive buffer fill rate means the source data rate is greater than the sink data rate. Thus, based on the buffer data level (claimed filling measurement) the controller portions the amount of source rate and sink rate (claimed write and read rate), thereby setting a ratio).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor

and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams as applied to claim 1-4, 6, and 9-10 above and further in view of EP 1067793 to Tanlyama et al. (Hereinafter Tanlyama)

As per claim 5, Williams teaches buffer management system as claimed in claim 1.

Williams is silent on: comprising a decompressor.

However, Tanlyama discloses, in Fig.3, box 17, a decoder used to decode/decompress audio/video frames.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include a decompressor in a communication system as suggested by Tanlyama. The benefit for the modification is to allow decoding of audio/video frames that have been encoded and compressed to reduce size and increase transmission speed.

Although Williams teaches a buffer management system (Fig. 1, Box 22, Data Rate Regulator) where a delay control component (Fig. 1, box 22, Data Rate Regulator), is arranged to control the data rate conversion component (Fig. 1, Box 38, Controller)

Williams is silent on: on the basis of a decompression delay associated with the decoder and/or an amount of data units are in a second buffer

However, Tanlyama discloses, in Paragraph 0006, that bit streams are digitally decoded by first estimating how high an occupancy level of the buffer will be when a first frame of each scene starts being decoded. If the estimated buffer occupancy level when a scene starts being decoded is less than a predetermined level by a deficit, then start of decoding a first frame of a first scene is postponed until data of the first scene has been stored in the buffer to a level equal to a sum of the deficit and the predetermined level. Thus, in the case where the buffer occupancy level has a shortage of data when a scene begins to decode, thereby incurring a decoding delay, the decoding will stop in order to fill the buffer occupancy level to a predetermined value, thereby controlling the read/write rate of the buffer. Also see Paragraph 0005.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to control a read/write rate by the decompression delay incurred by a decoder as suggested by Tanlyama. The benefit for the modification is to allow decoding of audio/video frames to produce seamless streaming of data at the receiver.

7. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams as applied to claim 1 above and further in view of the examiner.

As per claims 7-8 the examiner notes **a quotation from the MPEP under section 2114, which forms the basis for determining patentability of claims dealing with intended use:**

“Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim.” Ex

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parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). Furthermore, “[i]nclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims.” In re Young, 75 F.2d 996, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 312 F.2d 937, 136 USPQ 458, 459 (CCPA 1963)).

As per claim 7, the preamble “Headphones comprising” is an intended use and not further limited by the body of the claim: “a digital audio receiver as claimed in claim 6, an output of the digital audio receiver being connected to a loudspeaker of the headphones”.

Whereby the Digital Audio Receiver connected to a buffer management system claimed in claim 6 (anticipated by Williams) would have been obvious to use/apply towards “Headphones” (a communication device as anticipated by Williams, Col. 10, 40-47) to any one with ordinary skill in the pertinent art.

As per claim 8, the preamble “Stand-alone surround sound loudspeaker cabinet comprising” is an intended use and is not further limited by body of the claim: a digital audio receiver as claimed in claim 6, an output of the digital audio receiver being connected to a loudspeaker in the cabinet.

Whereby the Digital Audio Receiver connected to a buffer management system claimed in claim 6 (anticipated by Williams) would have been obvious to use/apply towards a “Stand-alone surround sound loudspeaker” (a communication device as anticipated by Williams, Col. 10, 40-47) to any one with ordinary skill in the pertinent art.

Conclusion

8. Prior arts made of record, not relied upon:

US 6067653 to Tsukagoshi et al. discloses a Data decoder and data decoding method

US 6766376 B2 to Harold Edward Price discloses a buffering system for streaming media.

US 5027351A to Martin L. F. De Prycker et al. disclose an asynchronous time division communication system for regulating buffer filling.

US 6965804 B1 to Laura Merics et al. disclose a buffer management system for digital audio

US 7111091 B2 to Ari Lakaniemi et al. disclose a device and method for controlling a stream of data packets.

US 6778499 B1 to Nimal G. Senarath et al. disclose a method and apparatus for handling bursty data in a communication system.

US 6598132 B2 to Toan D. Tran disclose a buffer manager for network switch port.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yosief Berhane whose telephone number is (571) 270-7164. The examiner can normally be reached at 7:30-5:00 Mon-Fri.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached at (571) 272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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